

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	10773948
Filing Date	2004-02-06
First Named Inventor	S. Babar Raza
Art Unit	2416
Examiner Name	Hahn N. Nguyen
Attorney Docket Number	CD02209

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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	1	Application Number 10/746,349 (CD02208): "Logic for Implementing a Dual Clock Domain Read Access with Predictable timing for Bi-Directional Inputs/Outputs;" Raza filed on 12/24/2003; 31 pages	<input type="checkbox"/>
	2	Provisional Application 60/445,872 (CD02208P): "Logic for Implementing a Dual Clock Domain Read Access with Predictable timing for Bi-Directional Inputs/Outputs;" Raza filed on 02/07/2003; 6 pages	<input type="checkbox"/>
	3	Provisional Application 60/437,303 (CD02209P): "Dual-Port Memory Using a Single Port Memory for Multiple Clock Domain;" Raza filed on 12/31/2002; 9 pages	<input type="checkbox"/>

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